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10/554,383	10/25/2005	Hendrikus Petrus Elisabeth Vranken	NL03 0461 US1	7931

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EXAMINER	
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ART UNIT	PAPER NUMBER
2117	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/554,383	VRANKEN ET AL.	
	Examiner	Art Unit	
	DANIEL F. MCMAHON	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,13,15 and 17-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,13,15 and 17-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1 – 9, 13, 15, and 17 - 21 are presented for examination.

Claims 10 - 12, 14, and 16 are cancelled.

Response to Argument

1. Objection to the drawings is withdrawn in light of the amendment to the drawings.

2. Objections to the specification:

Regarding the objection to the title the objection is withdrawn in light of the amendment to the specification.

Regarding the objection under rule 37 CFR 1.77 the objection is withdrawn in light of applicant's argument.

3. Regarding applicant's response to the 35 U.S.C. 112 rejection: The rejection is withdrawn due to applicant's amendment.

Regarding applicant's response to 35 U.S.C 102 rejections:

4. Applicant's argument regarding claims 1-3, 8-10, and 13-16 and Venkataraman has been fully considered and is not persuasive. Venkataraman does teach: merging n compatible vectors and then reconstructing the n vectors by filling in don't care bits using either a random fill process or a merge fill process (page 574, column 2, lines 16 – 18; page 576, Experimental Results), where selection between random fill and merge fill is based on the number n (page 575, Balancing Testcubes with Respect to

Polynomials, column 2, last paragraph; page 576, Balancing Testcubes with Respect to Polynomials, column 1, first paragraph).

Regarding applicant's response to 35 U.S.C 103 rejections:

5. Applicant's argument regarding claims 4 – 6, Distler and Venkataraman has been fully considered and is not persuasive. Venkataraman teaches: the selection and use of different fill methods based on the number of merged vectors (page 575, Balancing Testcubes with Respect to Polynomials, column 2, last paragraph; page 576, Balancing Testcubes with Respect to Polynomials, column 1, first paragraph). Therefor it is unnecessary for Distler to teach: the selection and use of different fill methods based on the number of merged vectors.

6. Applicant's argument regarding claim 7, 12, Wang, Distler and Venkatarman has been fully considered and is not persuasive. Venkatarman teaches: processes for filling don't care bits (page 574, column 2, lines 16 – 18; page 576, Experimental Results). Therefor it is unnecessary for Wang to teach: processes for filling don't care bits.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. Claims 1 – 21 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Regarding claim 1, the amended limitation: reconstructing said n vectors from the merged vector by filling in don't care bits using a selected one of a random fill process and a merge fill process, selection between random fill and merge fill being based on the number n is not supported in the specification. The specification discloses: reconstructing the care bits in the test vector data by repeating the merged vector one or more times according to its respective repeat value, applying the reconstructed test vector data to an input of the logic product, and obtaining the resultant output data (specification: page 5).

Prior Art Rejections

9. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims 1 – 3, 8, 9, 13, and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Venkataraman et al. (herein Venkataraman), "An Efficient Bist Scheme Based On Reseeding Of Multiple Polynomial Linear Feedback Shift Register".

12. Regarding claim 1, Venkataraman discloses: A method of compressing data comprising a sequence of at least two subsequent vectors (page 574, Compaction of Testcubes); wherein a vector comprises one or more bits including care bits and don't care bits, the method being characterized by the steps of: comparing corresponding bits of the two or more subsequent vectors to determine if they are compatible; responsive to determining that all corresponding bits of a number n of said two or more vectors being compatible, merging said n vectors to create a single vector representative thereof (page 574, Compaction of Testcubes); and reconstructing said n vectors from the merged vector by filling in don't care bits using a selected one of a random fill process and a merge fill process (page 574, column 2, lines 16 – 18; page 576,

Experimental Results), selection between random fill and merge fill being based on the number n (page 575, Balancing Testcubes with Respect to Polynomials, column 2, last paragraph; page 576, Balancing Testcubes with Respect to Polynomials, column 1, first paragraph).

13. Regarding claim 2, Venkataraman discloses: data comprising test vector data for use in testing a logic product, and the method includes generating or obtaining original test vector data (page 574, Compaction of Testcubes).

14. Regarding claim 3, Venkataraman discloses: the original test vector data is generated by means of an Automated Test Pattern Generation (ATPG) tool (page 572, paragraph 5).

15. Regarding claim 8, Venkataraman discloses: An apparatus for compressing data (page 574, Compaction of Testcubes; page 576, Experimental Results).

16. Regarding claim 9, Venkataraman discloses: Apparatus according to claim 8, wherein said data comprises test vector data for use in testing a logic product (page 573, paragraph 2).

17. Regarding claim 13, Venkataraman discloses: an apparatus according to claim 9, including , an Automated Test Pattern Generation (ATPG) tool to generate original test vector data (page 572, paragraph 5).

18. Regarding claim 15, Venkataraman discloses: a memory to store merged vectors for use in testing the logic product (figure 1).

19. Regarding claim 18, Venkataraman discloses: the random fill process is used when n is less than a specified number, otherwise the merge fill process is used (page 575, Balancing Testcubes with Respect to Polynomials, column 2, last paragraph; page 576, Balancing Testcubes with Respect to Polynomials, column 1, first paragraph).

20. Regarding claim 19, Venkataraman discloses: the comparing and merging steps are repeated, resulting in a plurality of merged vectors (page 574, Compaction of Testcubes).

Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Venkataraman as applied to claim 1 above, and in view of Distler et al. (herein Distler), U.S. Publication 2002/0099992.

22. Regarding to claim 4, Venkataraman teaches all the limitations of claim 1, as cited above. Venkataraman does not teach: generating a repeat value in respect of one or more merged vectors, said repeat value being indicative of a number of times the respective merged vector should be repeated to reconstruct the care bits in the vectors of which the merged vector is representative.

Distler teaches: generating a repeat value in respect of one or more merged vectors, said repeat value being indicative of a number of times the respective merged vector should be repeated to reconstruct the care bits in the vectors of which the merged vector is representative (paragraph 0026).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Venkataraman: compressing data comprising a sequence of at least two subsequent vectors, wherein a vector comprises one or more bits, the apparatus being characterized by (i) means for comparing corresponding bits of two or more data subsequent vectors to determine if they are compatible; and (ii) means for merging said two or more vectors in which all corresponding bits of said vectors are compatible, to create a single vector representative of said two or more vectors; wherein compatibility of two bits is achieved provided that they do not have specifically

incompatible or opposite values; with the teaching of Distler: generating a repeat value; for the purpose of increasing fault coverage of the compressed vector during test.

23. Regarding to claim 5, Venkataraman and Distler teach all limitations of claim 4, as cited above. Additionally, Venkataraman teaches: a data set comprising test vector data for use in testing a logic product (page 573, paragraph 2).

24. Regarding claim 6, Venkataraman and Distler teach all limitations of claim 5, as cited above. Venkataraman does not teach: reconstructing the test vector data by repeating the merged vector one or more times according to their respective repeat values, applying said reconstructed test vector data to an input of said logic product and obtaining the resultant output data.

Distler teaches: reconstructing the test vector data by repeating the merged vector one or more times according to their respective repeat values, applying said reconstructed test vector data to an input of said logic product and obtaining the resultant output data (paragraph 0026).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Venkataraman, as cited above for claim 1, 4, and 5; with the teaching of Distler: reconstructing the test vector data by repeating the merged vector one or more times according to their respective repeat values, applying said reconstructed test vector data to an input of said logic product and obtaining the

resultant output data; for the purpose of increasing fault coverage of the compressed vector during test.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Venkataraman and Distler as applied to claim 6 above, and further in view of Wang, Chiou, (herein Wang), "Generating Efficent Tests for Continious Scan".

1. Regarding claim 7, Venkataraman and Distler teach all the limitations of claim 6, as cited above, compressing two vectors, generating a repeat value, and reconstructing the compressed vectors. Venkataraman and Distler do not teach: compressing said output data. Wang does teach: compressing said output data (page 162, column 2, lines 10-11).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Venkataraman and Distler: the step of compressing said output data comprising a sequence of at least two subsequent output vectors, wherein an output vector comprises one or more bits, the method being characterized by the steps of: comparing corresponding bits of two or more subsequent ~ vectors to determine if they are compatible; and, responsive to determining that all corresponding bits of said output vectors are compatible, merging said two or more output vectors to create a single output vector representative thereof, with the teaching of Wang: compressing said output data, for the purpose of reducing the number of clock cycles required to scan out test results (Wang, page 162, column 2, lines 13-16).

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Venkataraman as applied to claim 1 above, and in view of Barnhart et al., (herein Barnhart), "OPMISR: The Foundation for Compressed ATPG Vectors".

25. Regarding claim 17, Venkataraman teaches all the limitations of claim 1. Venkataraman does not teach: the merge fill process proceeds by one or more of repeat fill or repetitive background data fill. Barnhart teaches: the merge fill process proceeds by one or more of repeat fill or repetitive background data fill (page 753, column 2, paragraph 4).

Claims 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Venkataraman, in view of Jas et al., (herein Jas), "Test Vector Decompression via Cyclical Scan Chains and Its Application to Testing Core-Based Designs".

26. Regarding claim 20, Venkataraman teaches all the limitations of claim 19. Venkataraman does not teach: the merged vectors are arranged in a sequence of merged vector sets, each merged vector set having a first merged vector and a last merged vector, the method further comprising ordering the merged vector sets so that the last merged vector of one merged vector set is compatible with the first merged vector of the subsequent merged vector set.

Jas teaches: the merged vectors are arranged in a sequence of merged vector sets, each merged vector set having a first merged vector and a last merged vector, the method further comprising ordering the merged vector sets so that the last merged vector of one merged vector set is compatible with the first merged vector of the subsequent merged vector set (page 460, column 1, paragraph 2 and 3).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Venkataraman, as cited for claim 19, with the teaching of Jas, a merged vector set compatible with the subsequent merged vector sets, for the purpose of reducing the amount of test data to be stored and the amount of hardware to support testing (page 459, column 1, lines 1 – 9)

27. Regarding claim 21, Venkataraman teaches all the limitations of claim 20. Venkataraman does not teach: merging the last merged vector of the one merged vector set with the first merged vector of the subsequent merged vector set.

Jas teaches: merging the last merged vector of the one merged vector set with the first merged vector of the subsequent merged vector set (page 460, column 1, paragraph 2 and 3).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Venkataraman, as cited for claim 19, with the teaching of Jas, merging compatible vector sets, for the purpose of reducing the amount of test data to be stored and the amount of hardware to support testing (page 459, column 1, lines 1 – 9)

Conclusion

28. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANIEL F. MCMAHON whose telephone number is (571)270-3232. The examiner can normally be reached on M-Th 8am-5pm(EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571)272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JACQUES H LOUIS-JACQUES/
Supervisory Patent Examiner, Art Unit 2117

Dfm
06/12/08